

ABSTRACT

A timing generation circuit can increase a maximum delay amount without changing the configuration of a timing memory. The timing generation circuit includes: a timing memory (TMM) 10 containing predetermined timing data; a plurality of down counters 20 for loading timing data output from the TMM and outputting a pulse signal at the timing indicated by the timing data; an address selection circuit 40 for specifying one or two TMM addresses by switching and outputting corresponding one or two timing data; a load data switching circuit 50 used when two timing data are output from the TMM, for loading the two timing data to the two down counters cascaded and outputting one timing pulse signal; and a timing data selection circuit 60 for selecting one of the pulse signals based on the one or two timing data output from the down counter.